AN100 What are nvSRAM

Abstract

Nonvolatile SRAM (nvSRAM) are easy to use, high performance memories which keep their data valid even at sudden power loss. This application note explains the basics of nvSRAM operation based on the example of serial SPI nvSRAM.

Introduction

The outstanding performance of nvSRAM is founded by its double array architecture and in the use of differential logic in each memory cell.

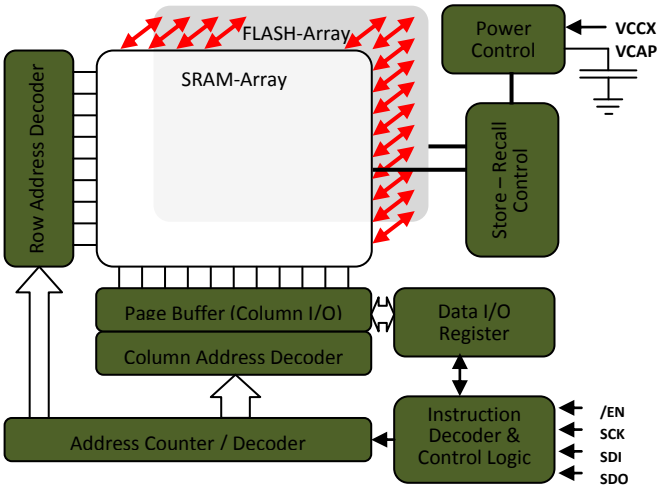

Figure 1: nvSRAM

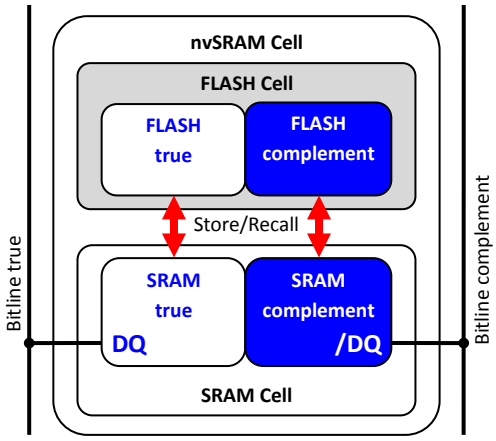

Figure 2: differential nvSRAM Cell

At Power-Up the SRAM-Array is automatically initiated with the data permanently stored in the Flash-Array.

All Read/Write operations are addressing the SRAM array only. From a user point of view, nvSRAM appears as ordinary SRAM. SRAM are fast, energy efficient and does not wear-out while R/W-operations. This explains the superior speed and the unlimited R/W endurance of nvSRAM.

The nonvolatile nature of nvSRAM is archived by Store operations copying the SRAM-Data to the shadow-Flash array. Using an extreme energy –efficient Flash technology and implementing a 1:1 connection, between each SRAM cell and its corresponding Flash cell, makes it possible to flip all SRAM data to the Flash array simultaneously in a single step operation.

Software – initiated Store operations get powered by the system power supply (VCCX).
VCC-monitoring-initiated Store operations (PowerStore) get powered by a small reservoir capacitor. The reservoir capacitor is charged at power-up and maintained during operation. This grants safe execution of PoweStore operations even in case of sudden and sharp power loss.

Recall operations copy an image of the Flash-Array to the SRAM array. Recall operations can be initiated any time by instruction.

Using differential logic speeds up all memory operation and improves noise immunity as well as data retention.

Anvo-Systems Dresden specific Features

In addition to the SPI standard instruction set, Anvo-Systems Dresden has implemented the following features:

Secure Write
Secure Write is an optional block transfer mode with checksum protected array access. The integrated online checksum generator calculates a checksum from the received address and data information and compares this checksum with a checksum received from the initiator of the data transfer. Transmission errors will be detected and indicated. Array access will be enabled only in case of correctly transferred address and data information.
SecureWrite benefits are:

- The correctness of data transfer can be monitored.
- Corrupt transferred data will not be stored.
- Corrupt transferred addresses can neither cause data loss nor overwrite existing data.

Secure Read
SecureRead is an optional block transfer mode generating a checksum from the received starting address and the transmitted data information. The initiator of the read access can recalculate the checksum and check if valid data has been received from the correct address.
For more details on SecureRead and SecureWrite see AN_201 Secure_RAM_Access.

Logging last Write Address
The address information of the last write access will be logged nonvolatile. This simplifies system recovery in case of sudden power loss.

Block and Page Rollover
Status Register bit 5 decides if continuous burst write operation will circle on the page buffer (like EEPROM) or write to the whole memory.

Recall last Stored Data
The double Array architecture makes it possible to distinguish between write and store. This means nvSRAM can withdraw written data and reload the last stored data to the SRAM array by executing a recall instruction.

Constraints of nvSRAM

Endurance
The number of nonvolatile Store operations of nvSRAM is limited to one million Store operations. This is comparable to the number of write operations of EEPROM or Flash. Since the number of Read

and Write operations of SRAM is not limited and Store operations are only needed at power down, the limitation in the number of Store operation is irrelevant for most applications.

Power-Up time
Booting the device and Initiating the SRAM Array with the Flash data at Power up takes about 550us. After this time Read/Write operations and Software Store are possible.

Charging the reservoir capacitor
The reservoir capacitor needs to be charged before PowerStore can be executed. Charging the reservoir capacitor takes about 5ms. For details see AN200_Reservoir_Capacitors.

Store execution time
While executing a Store operation, nvSRAM are busy for about 8ms and respond to status register read instructions only. This needs to be considered if software Store is used. PowerStore is executed at a time where the remaining system has already lost power. Store execution time is not critical in this case.

Configurations

To meet specific application needs, nonvolatile SRAM can be shipped in different configurations.

Part Number	Store Type	Reservoir Capacitor	Pinout 8-pin package
Anv31xxxxx	SoftStore	No	Standard
Anv32xxxxx	PowerStore	external	Pin#3 = VCAP
Anv33xxxxx	PowerStore	integrated	Standard
Anv35xxxxx	PowerStore	System Capacitance	Standard
Anv36xxxxx	Nonvolatile Write	no	Standard

Nonvolatile memories are ideal for the following applications:
Data logger, event data recorder, payment systems, axis logs of robots…

Version History

Revision	Date	Modifications
0.0	02.12.2011	initial version
0.1	29.08.2013	changed block diagram and minor changes

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