Migration from serial SPI EEPROM to serial SPI nvSRAM

Anvo-Systems Dresden nvSRAM fulfill exceptionally application needs by smart combination of two standard technologies, SRAM and SONOS-FLASH, in a double array architecture.

The SRAM array is used for standard operation. Unbeatable speed, R/W endurance and power consumption root in the fact, that all external access to the nvSRAM device is addressing the SRAM-array only.

The nonvolatile nature of nvSRAM is guaranteed by the integrated SONOS FLASH. At power up the FLASH initiates the SRAM in less than a millisecond. SRAM data can be saved to the FLASH under all operation conditions – even at sudden and sharp power loss. For this reason store operations can be powered by the energy stored in a small capacitor.

Existing applications using any kind of serial SPI nonvolatile memories can migrate to nvSRAM without or with minimal changes in hardware and firmware. The migration effort depends on the application needs and the specific type of nvSRAM used. For example Anvo-Systems Dresden offers nvSRAM with integrated capacitor. In this case no changes in hardware are needed.

This application note provides an overview about advantages and potential issues to be considered when migrating from serial SPI EEPROM to serial SPI nvSRAM, based on the comparison of nvSRAM to three examples of EEPROM.

The migration to nvSRAM may result in improved application performance. The best result can be archived if a new design makes advantage of all features and improved parameters of nvSRAM. The table below gives an overview about improvements to be expected in case of migration from serial SPI EEPROM to serial SPI nvSRAM.

	nvSRAM advantages in case of		
	new design	design in	drop in
Checksum protected array access (Secure Write)	++	++	o
Logging of last write address (RLSWA)	++	++	o
Two memory arrays in one device	+	+	o
Safe execution of last write instruction	+	+	+
Excellent data retention	++	++	++
Differential memory cell	+	+	+
Improved Speed	+	+	o
Unlimited R/W endurance	++	++	+
Lower price (must include storecap and board space)	o	o	o

New design: HW, firmware and application are designed to use nvSRAM features
Design in: HW and firmware are modified to use nvSRAM features
Drop in: no changes in HW and firmware

Standard Pin out and Access Protocol supports Migration

Migration between serial memories is simplified by the existing quasi-standards for serial memory pin out, instruction set and access protocol. In the best case the nvSRAM can replace the existing solution without any change.

On the other hand it is well known that memories feature product- and manufacturer-specific options and parameters. That's why the compatibility of hardware features, access protocol and device parameters needs to be checked carefully for each single case of migration.

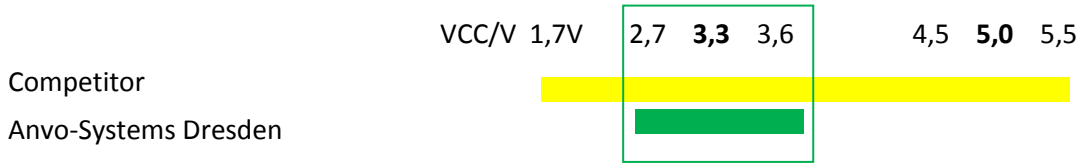
Some of the nvSRAM advantages, like exceptional write speed and unlimited endurance, root in the double memory array architecture. Each memory array is optimized for its specific task. This provides a better performance than a single array where compromises are needed. As a drawback the safe transfer of all SRAM - data to the FLASH need to be granted even if a sudden and sharp drop of the operating voltage occurs. This requires automatic execution of the nonvolatile STORE operation powered from an independent source of energy. Since AutoStore takes only little energy, a small capacitor loaded and maintained at normal operation is sufficient for this purpose. In general, this capacitor can be integrated into the package or connected via a separate pin. But, integrating the capacitor into the package causes additional process steps and high density capacitors. Therefore it is more expensive to integrate the capacitor than using an external capacitor.

Example Comparison of Parameters and Features

In many cases the application does not use the incompatible features. If, for example, the extended operation voltage range is not utilized by the application, devices with standard operation voltage can be used.

	Anvo-Systems Dresden	Microchip	ROHM	ON-Semi
Device	nvSRAM	EEPROM	EEPROM	EEPROM
Order Code	Anv32C81WSK	25AA256-I/SN	BR25S256FJ-WE2	CAT25256VI-G
Density	256Kb	256Kb	256Kb	256Kb
Configuration	32Kx8	32Kx8	32Kx8	32Kx8
Operating Temp.	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C	-40°C to 85°C
VCC	2.7V-3.6V	1.8V-5.5V	1.7V-5.5V	1.8V-5.5V
Package	SOIC8-150MIL	SOIC8-150MIL	SOIC8-150MIL	SOIC8-150MIL
Speed	66MHz	10Mhz	20MHz	20MHz
Endurance R/W	unlimited	10^6	10^6	10^6
Endurance STORE	10^6			
Data Retention	100years@55°C	200 years	40 years	100 years
Iccsb	200µA	1µA	2 µA	1 µA
ICCW	< 5mA@66MHz	< 5mA	<3mA (*3)	<4mA (*1)
ICCR	< 5mA@66MHz	< 6mA(*1)	<8mA(*3)	<2mA (*1)

Table 1: Compatibility of 256Kb nvRAM
(*1)VCC = 5.5V 10MHz
(*3)VCC = 5.5V 20MHz
Competitor devices feature extended voltage range. Always check voltage used in customer application.

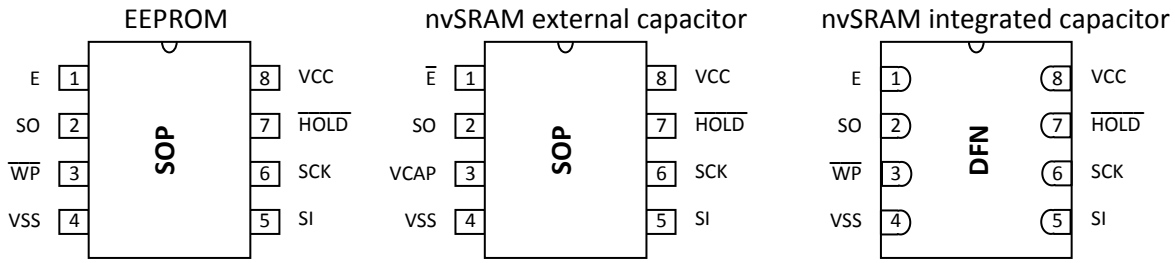


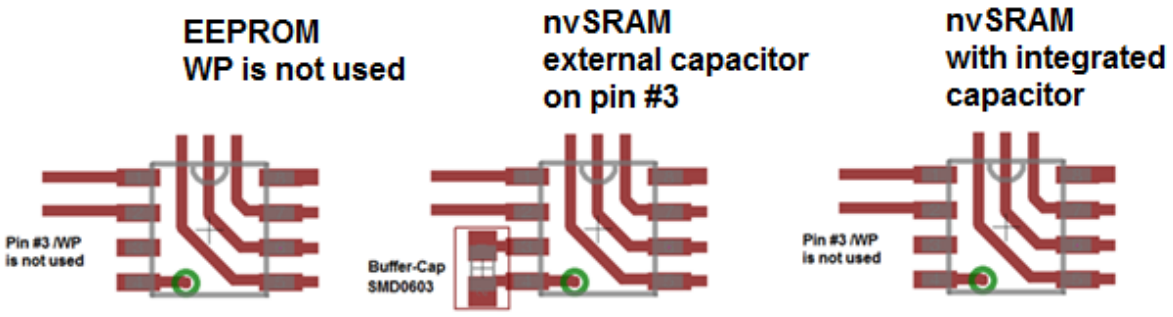
Competitors feature a whole zoo of different packages. Check footprints and available assembly equipment.

SOIC8-Pinout

	Anvo-Systems Dresden	Microchip	ROHM	ON-Semicoductor
Device	nvSRAM	EEPROM	EEPROM	EEPROM
Order Code	Anv32C81WSK	25AA256-I/SN	BR25S256FJ-WE2	CAT25256VI-G
Pin1	/E	/CS	/CSB	/CS
Pin2	SO	SO	SO	SO
Pin3	**VCAP**	/WP	/WPB	/WP
Pin4	VSS	VSS	GND	VSS
Pin5	SI	SI	SI	SI
Pin6	SCK	SCK	SCK	SCK
Pin7	/HOLD	/HOLD	/HOLDB	/HOLD
Pin8	VCC	VDD	VCC	VCC

If small 8-pin packages and an external capacitor are used, VCAP occupies the position of the Hardware Write Protect (WP) pin. This should not be an issue, because hardware write protect is typical not used. DFN8, the package used for nvSRAM with integrated capacitor fits the SOP8 footprint.





If the board layout includes the footprint for the capacitor at pin #3 (as shown on the center of the picture above), the following assembly options are possible.

Memory	Connected to pin #3	Comment
FRAM,MRAM,EEPROM, FLASH nvSRAM with integrated cap	none	Standard operation, no hardware write protect
FRAM,MRAM,EEPROM, FLASH nvSRAM with integrated cap	resistor	Standard operation, with option for hardware write protect
nvSRAM autostore ext. cap	storecap	Standard operation, no hardware write protect
nvSRAM softstore	none	Softstore operation , no hardware write protect
nvSRAM softstore	resistor	Softstore operation , with option for hardware write protect

PCB - Layout

In many cases hardware write protect is either not used at all, or used for issues (avoid useless high power consumption at unintended WRITE operation) which are fixed if nvSRAM are used.

Status Register Usage

	Anvo-Systems Dresden	Microchip	ROHM	ON-Semi
Device	Anv32C81WSK	25AA256-I/SN	BR25S256FJ-WE2	CAT25256VI-G
SR-Bit7	WPEN	WPEN	WPEN	WPEN
SR-Bit6	PDIS	x	0	IPL
SR-Bit5	PRO	x	0	-
SR-Bit4	/SWM	x	0	LIP
SR-Bit3	BP1	BP1	BP1	BP1
SR-Bit2	BP0	BP0	BP0	BP0
SR-Bit1	WEN	WEL	WEN	WEL
SR-Bit0	/RDY	WIP	/R/B	/RDY
BP1, BP0 = 00	none	none	none	none
BP1, BP0 = 01	6000h to 7FFFh	6000h to 7FFFh	6000h to 7FFFh	6000h to 7FFFh
BP1, BP0 = 10	4000h to 7FFFh	4000h to 7FFFh	4000h to 7FFFh	4000h to 7FFFh
BP1, BP0 = 11	0000h to 7FFFh	0000h to 7FFFh	0000h to 7FFFh	0000h to 7FFFh

ON-Semiconductor offers the extra feature „Identification Page“.
IPL: Identification Page Latch
LIP: Lock Identification Page

The nvSRAM status register is a superset of EEPROM status register. The additional status register bits can be ignored for EEPROM like operation.

- PDIS provides the option to disable automatic nonvolatile store operation.
- PRO enables continuous write operation exceeding page boundaries.
- /SWM informs about the success of an SecureWrite operation.

SPI Instruction Set

	Anvo-Systems Dresden	Microchip	ROHM	ON-Semi
Device	Anv32C81WSK	25AA256-I/SN	BR25S256FJ-WE2	CAT25256VI-G
WREN	0000 0110	0000 0110	0000 0110	0000 0110
WRDI	0000 0100	0000 0100	0000 0100	0000 0100
RDSR	0000 0101	0000 0101	0000 0101	0000 0101
WRSR	0000 0001	0000 0001	0000 0001	0000 0001
READ	0000 0011	0000 0011	0000 0011	0000 0011
WRITE	0000 0010	0000 0010	0000 0010	0000 0010
SECURE READ	0001 0011			
SECURE WRITE	0001 0010			
STORE	0000 1000			
RECALL	0000 1001			
RLSWA	0000 1010			
WRSNR	1100 0010			
RDSNR	1100 0011			
HIBERNATE	1011 1001			

Anv32C81WSK implemented all standard SPI-Instructions.

Page buffer width

Accessing memories arrays always reads or writes all data of one row (word line) to or from a local buffer. For serial SPI memories this buffer is called page buffer. In case of consecutive addressing block transfer modes can be used to improve interface speed and to reduce the number of array accesses. Since EEPROM suffer from ware out, efficient coding makes use of the page buffer.
The size of the page buffer is typically 32, 64 or 128 bytes and directly corresponds to the architecture of the memory array. If the size of the page buffers is different, the firmware may need to be adjusted.

Advantages of nvSRAM

Speed
By technology nvSRAM are the fastest nonvolatile memories at the market.
SPI Speed 66MHz vs. 40MHz

Unlimited R/W endurance
Wrong coded firmware can exceed the maximum number of write cycles for serial SPI EEPROM after a few hours. This means wear leveling need to be implemented. Since there is no wear mechanism for nvSRAM , the parts can safely be written without the need to implement and verify wear leveling.

SecureWrite
sensitive data cannot be overwritten by incorrect transferred address-information
prevents from data loss caused by incorrect transferred address-information
prevents from writing incorrect transferred data

RLSWA (logging of last write address)
Helps to repair systems after unexpected power down.
Can be used to simplify the implementation of circular buffers.

Two memory arrays in one device
Option to recall initial system state.

Safe execution of last write instruction
Autostore will interrupt last write access if the remaining system power is not sufficient to finish write access. No damaged data will be written to the memory. Autostore itself will run autarkic.

Excellent data retention
The used SONOS FLASH cell stores data in isolated charge traps. Aging of the SONOC structure will always affect only single charge traps. This improves the long term stability of the storage element.

Differential Store Cell
nvSRAM are using two storage elements to store one single bit. This improves the signal margin while reading.

nvSRAM offer attractive pricing
nvSRAM are using small feature size, standard technologies and only a few additional process steps. This results in cost effective production.

Migration Check List

Pin Configuration
Package dimensions
VCC compatible
Power consumption
Initiate and leave hibernate mode
Page width
Temperature range
SPI-Speed
SPI-Instruction Set
Status register usage
Block protection areas

Version History

Date	Version	Changes
27-November 2012	1.0	Initial version