Migration from serial SPI FRAM to serial SPI nvSRAM

Anvo-Systems Dresden nvSRAM are fast and reliable non-volatile memories built by conventional CMOS technology in double array architecture. In most cases nvSRAM can replace emerging memories like FRAM or even MRAM. Using nvSRAM can even improve the application performance.

This application note provides an overview about advantages and potential issues to be considered when migrating from serial SPI FRAM to serial SPI nvSRAM. Figure1 shows the block diagram of serial SPI FRAM and nvSRAM.

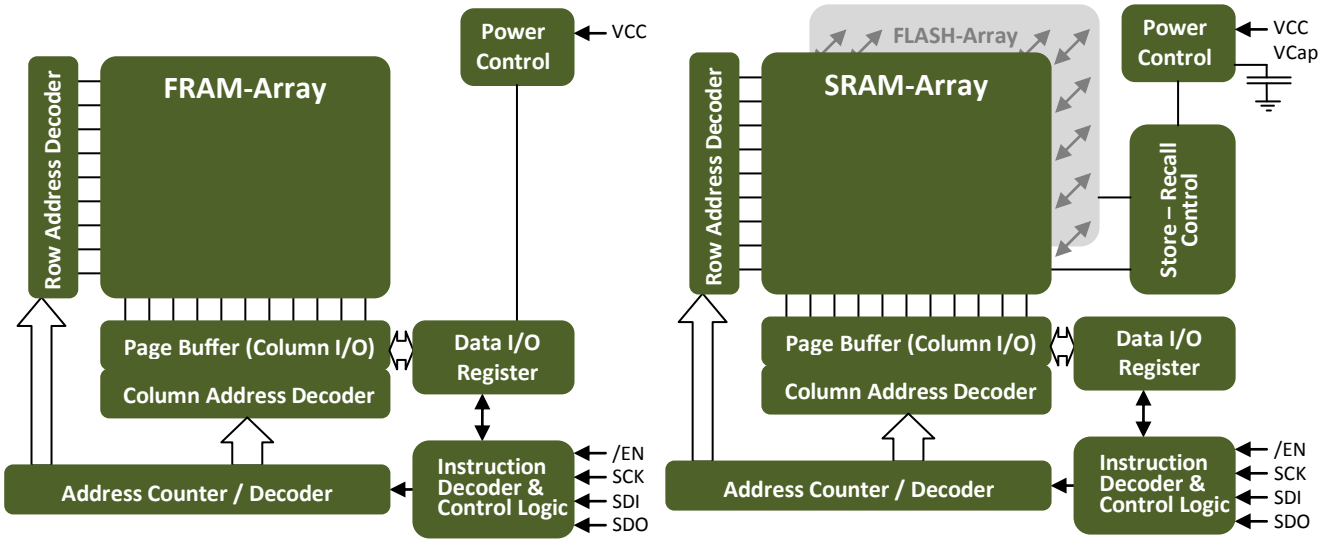
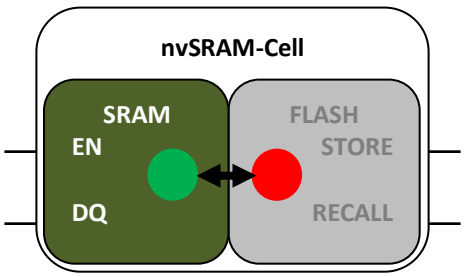


Figure1. Block Diagram FRAM nvSRAM

The nonvolatile nature of nvSRAM is guaranteed by the integrated SONOS FLASH. At power up the FLASH initiates the SRAM in less than a millisecond. SRAM data can be saved to the FLASH under all operation conditions – even at sudden and sharp power loss. For this reason store operations can be powered by the energy stored in a small capacitor.



Each SRAM-cell is directly connected to its corresponding SONOS Flash-cell. Automatically at power-up, or explicitly on SPI-Instruction, all SRAM-cells will be initiated with the data stored in the Flash.
On power-down, or explicitly on SPI-Instruction, SRAM-data can be saved to the Flash-cell.
Programming SONOS Flash is as energy- efficient, as that a small reservoir capacitor, charged at power-up, is sufficient to provide the energy needed to backup the whole SRAM array to the FLASH independent from the state of the system power supply.

FRAM need to combine the conflicting volatile and nonvolatile characteristics of high speed nonvolatile memories in a single memory array. In difference, nvSRAM feature double array architecture with an SRAM array, optimized for fast and reliable volatile operation and an SONOS-Flash array, optimized for reliable energy efficient nonvolatile operation. The external interface of an nvSRAM is addressing the SRAM-array only. This makes the superior nonvolatile characteristics of SRAM, such as speed and unlimited endurance, available for the user.

Standard Pin configuration and Access Protocol supports Migration

Migration between serial memories is simplified by the existing quasi-standards for serial memory pin out, instruction set and access protocol. In the best case the nvSRAM can replace the existing FRAM without any change. On the other hand it is well known that memories feature product- and manufacturer-specific options and parameters. For this reason the compatibility of hardware features, access protocol and device parameters needs to be checked carefully for each single case of migration.

Standard Pin Configuration

Eight-pin packages (SOIC, DFN) are very popular for non-volatile memory with SPI interface.
The standard pin configuration for nonvolatile memories with SPI-Interface utilizes all eight pins.

Pin#	Function	FRAM	Anv31xxx	Anv32xxx	Anv33xxx	Anv35xxx
			Softstore	AutoStore Ext. Cap	AutoStore Int. Cap	AutoStore Syst.Cap
1	Chip Enable	/S	/E	/E	/E	/E
2	Serial Output	Q	SO	SO	SO	SO
3	Write Protect	/W	/W	**VCAP**	/W	/W
4	Ground	VSS	VSS	VSS	VSS	VSS
5	Serial Input	D	SI	SI	SI	SI
6	Serial Clock	C	SCK	SCK	SCK	SCK
7	Hold	/HOLD	/HOLD	/HOLD	/HOLD	/HOLD
8	Ground	VDD	VCC	VCC	VCC	VCC

Table 1. Pin configuration FRAM compared to different nvSRAM configurations

Anvo-Systems Dresden nonvolatile SRAM can be configured for different store options. Possible configurations are listed in Table 1. The most popular configuration (Anv32xxx) is capable of executing self – sufficient automatic store operations powered by cost-efficient external reservoir capacitors. This package utilizes pin #3 to connect the external capacitor. In this configuration Hardware Write Protect is not available. Figure 2 shows a schematics f

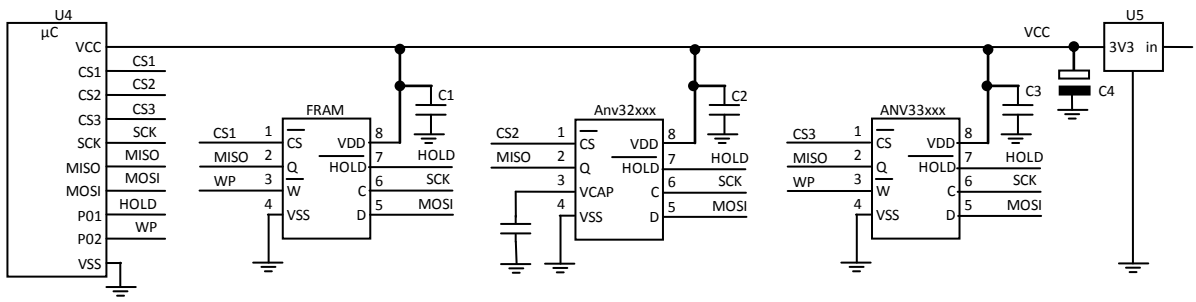


Figure 2: FRAM, PowerStore nvSRAM with external and internal reservoir capacitor.

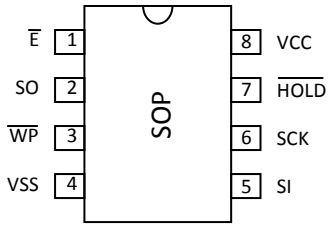
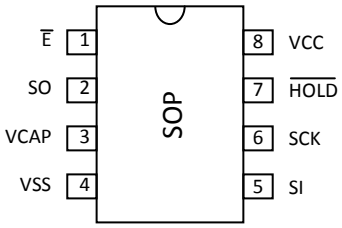
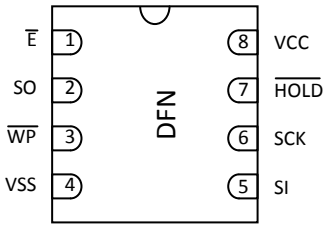
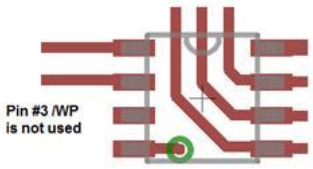
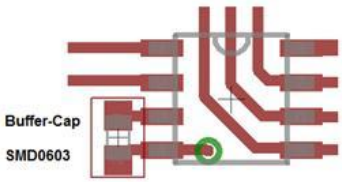
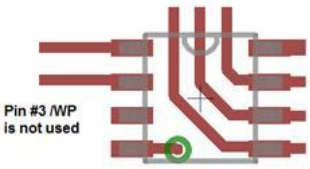
FRAM	nvSRAM external capacitor	nvSRAM integrated capacitor
		
/WP is not used	External capacitor on pin#3	Integrated capacitor
		

Table 2. FRAM and nvSRAM pin configuration – package, schematics and board layout.

Status Register Usage

The nvSRAM status register is a superset of the FRAM status register. Basic functionality of nvSRAM status register is the same as for FRAM. Table 2 shows the utilization of status register bits for nvSRAM and some example FRAM. The extended functionality of Anvo-Systems nvSRAM is reflected in the introduction of additional status register bits.

- PDIS provides the option to disable automatic nonvolatile store operation.
- PRO enables continuous write operation exceeding page boundaries.
- /SWM informs about the success of a SecureWrite operation.
- /RDY is set if the device is busy. In FRAM like operation the device is always ready.

For FRAM-compatible device operation there is no need to change/evaluate the additional status register bits.

SR-Bit	Anv32C81	MB85RS256	FM25V02	FM25W	Comment
7	WPEN	WPEN	WPEN	WPEN	
6	PDIS	-	-	-	Disabled by default
5	PRO	-	-	-	Disabled by default
4	/SWM	-	-	-	Read only
3	BP1	BP1	BP1	BP1	
2	BP0	BP0	BP0	BP0	
1	WEN	WEL	WEN	WEN	
0	/RDY	-	-	-	can be ignored

Table 2. Utilization of status register bits

SPI Instruction Set

All serial SPI memories support a standard instruction set. Additional features may result in additional SPI-Instructions. Table 3 lists the standard and optional Instructions for nvSRAM and example FRAM. The absence of OP-Code conflicts is essential for migration.

SPI-OP-code	Anv32C81	MB85RS256	FM25V02	FM25W	Class
0000 0110	WREN	WREN	WREN	WREN	Standard
0000 0100	WRDI	WRDI	WRDI	WRDI	Standard
0000 0101	RDSR	RDSR	RDSR	RDSR	Standard
0000 0001	WRSR	WRSR	WRSR	WRSR	Standard
0000 0011	READ	READ	READ	READ	Standard
0000 0010	WRITE	WRITE	WRITE	WRITE	Standard
1011 1001	Hibernate	-	SLEEP	-	Optional
0000 1011			FSTRD	-	Optional
1001 1111		-	RDID	-	Optional
1100 0011	RDSNR	-	SNR	-	Optional
0001 0010	SECURE WRITE	-	-	-	Optional
0001 0011	SECURE READ	-	-	-	Optional
0000 1000	STORE	-	-	-	Optional
0000 1001	RECALL	-	-	-	Optional
0000 1010	RDLSWA	-	-	-	Optional
1100 0010	WRSNR	-	-	-	Optional

Table 3. SPI Instructions

Hardware Write Protect

FRAM inherited hardware write-protect from conventional nonvolatile memories like Flash or EEPROM. These memories execute a time- and power-consuming programming cycles after each Write instruction. While these programming cycles are running, the memory is busy and cannot execute Read or Write instructions. Neither FRAM nor nvSRAM execute this kind of programming cycle after Write instructions. On the other hand FRAM read destructive. This means even after reading from a write protected sector, the FRAM must write back the data into the write protected sector. But the feature exist and since some nvSRAM internally disable hardware write protect to free up pin #3 (/WP) to connect the reservoir capacitor (VCAP), this section will discuss more in detail how hardware write protect is working and what it can be used for.
Hardware write protect is using a simple mechanism to offer quite a lot of flexibility in write protection. This mechanism is: If /WP is tied to low AND status register bit #7 (WPEN) is set to high, then it is no longer possible to modify the status register. This means even the WPEN – bit in the status register cannot be reset once hardware write protect is activated. Figure 3 shows the logic circuit for this function. Hardware write protect is self-locking as long as /WP is low. The flexibility comes from the different status register contents and the different ways to control the /WP pin.

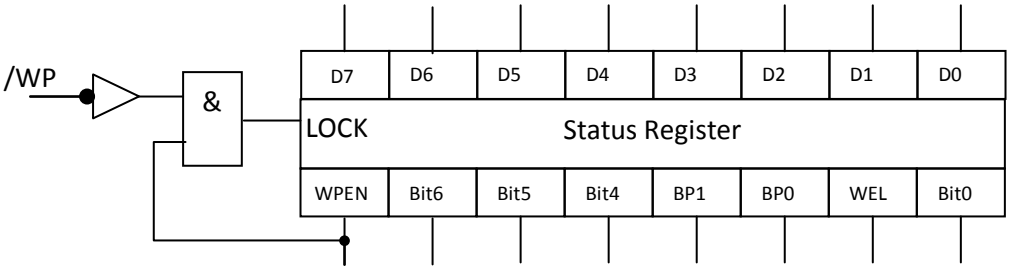


Figure 3. Hardware Write Protect

The benefits from using hardware write protect for FRAM are limited. That's why the /WP pin is typically tied to High. In case hardware write protect is not used FRAM can be replaced by nvSRAM with external reservoir capacitor. Potential use of hardware write protect is explained in the use cases below.

Use case 1 - /WP hard wired to GND
The status register becomes write protected as soon as status register bit #7 (WPEN) is set. The WPEN-bit in the status register is basically the "fuse" which can be burned to freeze the configuration of a device for example before shipment. This approach is suited to prevent the memory from unintended write access, but since the /WP-pin can be lifted up easily, this method is not suited for temper protection.

Use case 2 - /WP connected to a microcontroller port.
By changing the level on the /WP pin, the microcontroller can determine the time where the status register becomes prevented from unintended modifications. In order to enable or disable write access to the memory array, the microcontroller need to modify the block protection bits (BP1, BP2) as well. This is basically a two step microcontroller controlled software write protect.

No use case - /WP connected to a battery sensor.
To some respect it would be desirable to disable write access if a specific application is powered by battery, or if a battery-powered application is suffering from low battery voltage. But, in difference to the suggestion, hardware write protect just take care for the status register. In order to change write protection for the array, the block protection bits in the status register need to be modified by the microcontroller as well.

Software Write Protect

Unintended execution of write instructions may not just violate data consistency. Even unintended write instructions on EEPROM and Flash initiate a programming cycle of some milliseconds. The devices are busy for this time and neither responds to neither read instructions nor execute further write instructions. This can be inacceptable for applications. To avoid unintended execution of write-instructions, all serial SPI nonvolatile memories feature automatic write protection on device level.

This write protection must explicitly be deactivated by execution of a write-enable (WREN) instruction in front of any attempt to write either to the status register or to the memory array.

The WREN instruction sets the write enable latch in the status register. The execution of a Write instruction resets the write enable latch. It must be set again before executing the next Write instruction.

Block protection offers a second level of Write protection. The state of the block protection bits (BP0, BP1) in the status register defines if parts or the whole memory array are write-protected.

Protected Block	BP1	BP0
none	0	0
Upper quarter	0	1
Upper half	1	0
Whole memory	1	1

Table 4. Block protection bits

The procedure used to overcome software write protect is shown in Table 5.

Step	Write Protection Level	
	Device	Array
Set write enable latch by WREN-instruction	protected	protected
Write status register to clear block protection bits	free	protected
Set write enable latch by WREN-instruction	protected	free
Write data to memory array	free	free
Set write enable latch by WREN-instruction	protected	free
Write status register to set block protection bits	free	free
Next step	protected	protected

Table 5. Instruction sequence to access software write protected memories

This two level write protection provides a reasonable protection against unintended write access.

Secure Write on Anvo-Systems Dresden nvSRAM

Anvo-Systems Dresden nvSRAM feature a sophisticated option to prevent the memory from unintended write operations and from write access with corrupt data or address information. SecureWrite implements full speed checksum protected array access and monitors the status of the data transfer. The initiator of a write operation will see if the data has been correctly transferred to the specified address or have been refused by the nvSRAM to avoid writing corrupt data.
For more details on Secure Write see AN201 “Secure Ram Access”.

Specific Migration Remarks

While nvSRAM provide the same functionality as FRAM, they are based on different technology and feature different parameters and operation conditions. In many cases this differences will have no effect on existing applications. Table 6 lists the main differences which need to be checked to ensure proper migration.

Function	FRAM	Anv31xxx SoftStore No Cap	Anv32xxx PowerStore Ext. Cap	Anv33xxx PowerStore Int. Cap	Anv35xxx PowerStore Syst. Cap
Pin Configuration	standard	standard	Pin#3 VCAP	standard	standard
Package dimensions	various	SOIC8 150	SOIC8 150	MLP5x6	SOIC8 150
Hardware Write Protect	yes	yes	no	yes	yes
Power up to first read	250us	150us	150us	150us	150us
Power up to first write	250us	150us	5ms	5ms	150us
VCC stable after last access (with VCC>2V)	0 ms	8ms	0ms	0ms	8ms*[1]
Automatic Store at Power down	Write = Store	instruction store only	yes	yes	yes
R/W Endurance	10^{10} to 10^{14}	unlimited	unlimited	unlimited	unlimited
Power cycles	unlimited	10^6	10^6	10^6	10^6
VCC =2,7V… 3,6V	Yes	yes			
VCC = 2,7V … 5,5V	Yes	**no**			
SPI-Speed	40MHz	66MHz			
Standby power consumption	15uA	200uA			
Active power consumption	2mA@20MHz	2mA@10MHz, 5mA@66MHz			

Standard SPI Instruction Set	yes	yes	yes	yes	yes
Extended SPI Instruction Set	(No)	yes	yes	yes	yes
Unique Serial Number	(8byte)	(2 byte user programmable)			
Device ID	(Yes)	No	no	no	no
H/L on /CS stops sleep mode	(yes)	(yes)	(yes)	(yes)	(yes)
Temperature range	industrial	industrial	industrial	industrial	industrial
Status register bit 0	Not used	/RDY	/RDY	/RDY	/RDY
Status register bit 4	Not Used	/SWM (Secure Write Monitoring)			
Status register bit 5	Not Used	/PRO (Page rollover)			
Status register bit 6	Not Used	PDIS (Power store Disable)			
Standard SPI Instruction Set	yes	yes			
Extended SPI Instruction Set	(No)	yes			
Secure Write, Secure Read	no	Yes			

Table 6. migration-relevant features and parameters
() values in brackets are not applicable for all devices
*[1] slew rate Vcc limited

Example Comparison of Parameters and Features

Company	Anvo-Systems	Fujitsu	Ramtron	Ramtron
Device	Anv32C81W	MB85RS256A PNF-G-JNE1	FM25V02-GTR	FM25W256-GTR
	nvSRAM	FRAM	FRAM	FRAM
Size	256Kb	256Kb	256Kb	256Kb
Speed	66MHz	25MHz	40MHz	20MHz
VCCmin	2,7V	3V	**2,0V**	2,7V
VCCmax	3,6V	3,6V	3,6V	**5,5V**
Temperature Range	-40°C … +85°C	-40°C … +85°C	-40°C … +85°C	-40°C … +85°C
Endurance	Unlimited	10exp10	10exp14	10exp14
Data Retention	100years @+55°C	10years @+55°C	10 Years	38yers @+75°C
ICC max	5mA@66MHz	5mA @25MHz	2,5mA@40MHz	2mA@20MHz
Standby current	200uA	9uA	150uA	30uA
Package	SOIC8 – 150Mil DFN5x6	SOIC8 – 150Mil	SOIC8 – 150Mil TDFN8	SOIC8 – 150Mil
Power-Up time	5ms	**85ns**	**250us**	10ms
Power-Down time	0us	85ns	0us	0us
Standard SPI OP-Codes	WREN, WRDI, RDSR,WRSR, READ, WRITE	WREN, WRDI, RDSR, WRSR, READ, WRITE	WREN, WRDI, RDSR, WRSR, READ, WRITE	WREN, WRDI, RDSR, WRSR, READ, WRITE
Extended SPI Op-Codes	SECURE READ, SECURE WRITE, STORE, RECALL RLSWA, WRSNR, RDSNR, HIBERNATE	- none-	**FSTRD**, SLEEP, **RDID**, SNR	- none-

Table 7. Compatibility of 256Kb nvRAM

Migration Check List

- Pin Configuration
- Package dimensions
- VCC compatible
- Power consumption
- Initiate and leave hibernate mode
- Page width
- Temperature range
- SPI-Speed
- SPI-Instruction Set
- Status register usage
- Block protection areas

Summary

Replacing FRAM by nvSRAM can improve speed and reliability of applications. Standard Pin configurations and SPI instruction set simplifies the migration. Different ranges of operating conditions need to be considered but will typically not be gating for a specific migration.

Version History

Date	Version	Changes
15-August - 2012	1.0	Initial version
27-August - 2012	1.1	Added layout storecap
13-September-2012	1.2	Added integrated capacitor
29-May - 2013	1.3	Added Hardware Write Protect
29-May - 2014	1.4	Minor changes